Design and Optimization of Half Subtractor Circuits for Low-Voltage Low-Power Applications

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ABSTRACT
In this paper, we propose a leakage reduction technique. Because high leakage currents in deep submicron regimes are becoming a major contributor to total power dissipation of CMOS circuits. Sub threshold leakage current plays a very important role in power dissipation. So to reduce the sub threshold leakage current we proposed transistor gating. In this technique two sleep transistor PMOS and NMOS are inserted in between supply voltage and ground. During standby mode both these two sleep transistor are turned off therefore these transistor increase resistance of the path from Vdd to ground. By applying this technique we have reduced the leakage current from 7.413pa to 2.844pa and power from 2.348pw to 1.459pw. That means this technique reduce the leakage current 41.4%. The circuits is simulated on cadence virtuoso in 45nm CMOS technology. Simulation results revealed that there is a significant reduction in leakage current for this proposed cell with circuit reducing the supply voltage.

Keywords: Low-power design, Leakage power consumption, leakage current, half subtractor, sleep transistor.

1. INTRODUCTION
As a result of scaling, power dissipation due to leakage currents has increased dramatically and is a major source of concern especially for low power applications. Till now, the dominant leakage mechanism has been due to drain-source sub-threshold current. Assuming this leakage mechanism, a number of techniques have been proposed in literature for reducing the impact of leakage power dissipation such as gated-VDD scheme [1, 2], Dual-Vth SRAM [3] etc. With scaling of channel length, oxide thickness also needs to be scaled to maintain proper operation of MOS transistor. As a result, even though supply voltage has been reduced with new generations of technology, the magnitude of gate leakage current has increased steadily and is likely to become comparable or even larger than the sub-threshold leakage for future CMOS devices [4]. With the perspective that leakage power dissipation in logic circuit would constitute a significant fraction of overall power dissipation, an analysis of leakage currents in a half subtractor has been carried out and techniques for suppressing it are compared. Most of the techniques that have been proposed in the last few years to lower the sub-threshold leakage and gate leakage in logic and combinational circuits use reduced effective supply voltage.
to circuit during the inactive state. A few change the transistor substrate bias voltages during the inactive state. These techniques are associated with long wake-up latency when circuit changes from inactive state to active state and larger dynamic power dissipation when circuit changes from one state to another state. Low leakage asymmetric cells that reduce sub threshold leakage currents were proposed by N.Azizi etal., [5,6]. Power consumption is a major concern in the VLSI circuit design, for which CMOS is the primary technology. High power consumption leads to reduction in battery life in the case of battery powered applications and affects the reliability of the system. Power consumption of CMOS consists of dynamic and static component. Dynamic power is consume when transistors are switching. Components of static power dissipation are junction leakage, sub-threshold leakage, gate oxide leakage. As the technology continue to scale down a significance portion of the total power consumption in high performance digital circuits is due to leakage current because of reduced threshold voltage and device geometry. Therefore leakage Power reduction becomes the key to a low power design. The leakage or static power dissipation is the power dissipated by the circuit when it is in standby mode and is given by (1) Where is the leakage current that flows in a transistor in OFF state and VDD is the supply voltage. Leakage current consists of various components. Such as sub-threshold leakage, gate leakage, reverse– biased junction leakage, gate induced drain leakage, among these sub threshold leakage and gate leakage are dominant [8].

1.1 Source of leakage power

There are four main sources of leakage current in a CMOS transistor. This is shown in figure1.

Reverse-biased junction leakage current ($I_{REV}$)

Gate induced drain leakage ($I_{GIDL}$)

Gate direct-tunneling leakage ($I_G$)

Subthreshold (weak inversion) leakage ($I_{SUB}$) as described next.
1.1.1 Junction Leakage

The junction leakage occurs from the source or drain to the substrate through the reverse biased diodes when a transistor is OFF. A reverse-biased pn junction leakage has two main components: one is minority carrier diffusion/drift near the edge of the depletion region; the other is due to electron-hole pair generation in the depletion region of the reverse-biased junction [7]. For instance, in the case of an inverter with low input voltage, the NMOS is OFF, the PMOS is ON, and the output voltage is high. Subsequently, the drain-to-substrate voltage of the OFF NMOS transistor is equal to the supply voltage. This results in a leakage current from the drain to the substrate through the reverse-biased diode. The magnitude of the diode’s leakage current depends on the area of the drain diffusion and the leakage current density, which is in turn determined by the doping concentration.

1.1.2 Gate-Induced Drain Leakage

The gate induced drain leakage (GIDL) is caused by high field effect in the drain junction of MOS transistors. For an NMOS transistor with grounded gate and drain potential at VDD, significant band bending in the drain allows electron-
hole pair generation through avalanche multiplication and band-to-band tunneling. A deep depletion condition is created since the holes are rapidly swept out to the substrate. At the same time, electrons are collected by the drain, resulting in GIDL current. This leakage mechanism is made worse by high drain to body voltage and high drain to gate voltage. Transistor scaling has led to increasingly steep halo implants, where the substrate doping at the junction interfaces is increased, while the channel doping is low. This is done mainly to control punch-through and drain-induced barrier lowering while having a low impact on the carrier mobility in the channel.

### 1.1.3 Subthreshold Leakage

Subthreshold (or weak inversion) conduction current between source and drain in a MOS transistor occurs when gate voltage is below $V_{th}$ [12]. In the weak inversion, the minority carrier concentration is small, but not zero. Weak inversion typically dominates modern device off-state leakage current due to the low $V_{th}$. The weak inversion current can be expressed as [12], equation (1).

\[
I_{ds} = \mu_0 C_{ox} \left( \frac{W}{L} \right) (m - 1)(Vt)2e^{\frac{V_g-V_{th}}{mVt}}(1-e^{-Vds/Vt})
\]

Where $m = 1 + C_{dm}/C_{ox}$

### 1.2 Basic Half-Subtractor Circuit

A basic HS circuit consists of 18 transistors, in which 9 nMOS and 9 pMOS are used. A half subtractor is a combinational logic circuit that subtracts one bit from another. This circuit has two inputs, the minuend and the subtrahend bits, and two outputs the difference and borrow bits.

![Figure 2. Logic Symbol of Half Subtractor](image)
The truth table shown in Table 1 is constructed from the binary arithmetic operations. A practical use of half subtractor is for full subtractor in a digital system. Figure 2 shows the logic symbol of half subtractor. A basic half subtractor is made of a NOT gate, an AND and an XOR gate.

Table 1: Truth Table of half Subtractor

<table>
<thead>
<tr>
<th>Configuration</th>
<th>X</th>
<th>Y</th>
<th>D</th>
<th>B</th>
</tr>
</thead>
<tbody>
<tr>
<td>C0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>C1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>C2</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>C3</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
Fig(3). Basic half subtractor in transistor level

Here we can see that there are two inputs A and B and two outputs O/P1 and O/P2. Table (1) shows the truth table of Half subtractor design. Figure 3 shows the transistor level half subtractor design circuit. We can see, there are total ‘18’ transistors used to implementing the circuit, in which ‘9’ are PMOS transistors and rest of ‘9’ are NMOS transistors.

1.2.1 AND Gate
The AND gate is a basic digital logic gates that implements logical conjunction- it behaves according to the truth table to the right. A high output (1) results only if both the inputs to the AND gate are high (1). If neither or only one input to the AND gate is high, a low output results. In another sense, the function of AND effectively finds the minimum between
two binary digits, just as the OR function finds the maximum. Therefore, the output is always 0 except when all the inputs are 1s.

Fig(4). AND gate in Transistor level

Fig(4.1). Symbolic AND gate
Table 2. Truth table of AND gate

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

1.2.2 INVERTER

Inverter is designed by using one NMOS and one PMOS transistor. PMOS transistor works as pull-up network and NMOS transistor works as a pull-down network. In this combination PMOS transistor is connected to power supply and NMOS transistor is connected to ground. Fig (5) shows an inverter designed using CMOS logic gate. Further fig (6) shows a transistors level inverter design.

Fig (5). Inverter in transistor level

Fig (5.1). Inverter in symbolic
2. REVIEW OF PREVIOUS WORK
This section reviews different approaches for sub-threshold leakage current reduction techniques. A technique for leakage power control is Power gating [2][3], which turns off the devices by cutting off their supply voltage. This technique uses additional transistors (sleep), which are inserted in series between the power supply and pull-up network (PMOS) and/or between pull-down (NMOS) network and ground to reduce the standby leakage currents. The sleep transistors are turned on when circuits are in active mode and turned off when circuits are in standby mode. The multi-threshold voltage CMOS (MTCMOS) [4] technique is also a kind of power gating technique which uses high threshold transistors as a sleep transistors and low threshold voltage transistors are used to implement the logic. In dual threshold voltage CMOS technique [7], transistor of different threshold voltages are used. Low threshold voltage transistors are used for the gates on the critical path to maintain the performance, while high threshold voltage transistors are used for the gates on the non-critical path for reduction of the leakage current. Stacking effect has been defined in [6], when more than one transistor in the stack is turned off, stacking of series connected transistors used for the reduction of the sub-threshold leakage currents. This effect is called the. Forced stacking [5] yields the stacking effect by inserting extra transistor for every input of the gate in both PMOS and NMOS networks. So in the forced stacking two transistor are always off for every off input of the gate, which reduced the leakage current.

3. PROPOSED TECHNIQUE
In this paper a new technique of leakage reduction - “TRANSISTOR GATING TECHNIQUE” has been introduced. In this technique leakage current is reduced by inserting extra sleep transistors between power supply and ground. As shown in the figure 3 an PMOS sleep transistor (s) is inserted in between pull-up network and the network output and an NMOS sleep transistor (s’) is inserted in between the pull-down networks and the ground. During active mode, both sleep transistors are turned on by applying proper gate input voltage i.e. high (0.7v) for NMOS and low(0v) for PMOS, to reduced the resistance of the conducting paths from power supply to ground,
Fig(6). Proposed half subtractor circuit

thereby reducing performance degradation. During standby mode, both sleep transistors are turned off by applying proper

gate input voltage i.e. low(0v) for NMOS and high(0.7) for PMOS to produce stacking effect which reduces leakage

current by increasing resistance of the path from power supply to ground. The size of the existing transistors are set in

according to [1] shown in figure 5 and the size of the sleep transistors are set as W/L=1 with the P/N =2.

4. SIMULATION AND RESULTS

A half subtractor CMOS circuit is designed using 45 nm process technology. The proposed leakage reduction technique
called transistor gating is applied on this circuit as shown in Figure 4. The static power consumption associate with each
input vector, standby power are computed on Cadence Virtuoso Schematic Editor and Spectre tools. The results are shown in Table I. From the results as shown in Table I, in the active mode the static power consumption in the modified circuit is slightly less than the power consumption in base circuit for each input combination. But during the standby mode when both the sleep transistors are turned off in the modified circuit, the static power consumption is reduced up to the 40% in comparison to the static power in active mode for different input combination.

**Fig(7). Leakage current waveform of basic half subtractor**

**Fig(8). Leakage current waveform Proposed half subtractor**
Fig(9). Input Output waveform of Half Subtractor

Fig(10). Comparison leakage current of basic circuit and proposed circuit

Fig(11). Comparison of leakage power of base and proposed circuit
In the input vector 0 (low) represent 0 volt and 1(high) represent 0.7 volt. Also the power supply for this technology is 0.7 volt. In the active mode both sleep transistors are turns on by applying proper gate input, low input voltage for PMOS and high input voltage for NMOS. And during the standby mode both sleep transistor are turned off by applying high gate input voltage to PMOS and low gate input voltage to NMOS.

5. Conclusion
Simulation results demonstrated the reduction in power dissipation by using transistor gating. The results show a reduction in leakage current and leakage power compared to previously available models. For designing of half subtractor using 45 nanometer technologies reduces power consumption. In the proposed half subtractor leakage current reduce from 7.124pa to 2.844pa, and power consumption from 2.348pw to 1.459pw. It is 60% minimum leakage in compare to conventional half subtractor and power consumption 40% less as compare to conventional as we saw in fig.7 and fig.8.

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REFERENCES