ASIC Implementation of CDMA Transmitter using VHDL

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Abstract: In this paper direct sequence spread spectrum principle based code division multiple access (CDMA) transmitter has been designed in VHDL for FPGA. The main target is to design the transmitter circuit consisting of user data signal, PN sequence generator (gold code), BPSK modulator block. The primary objective for designing the CDMA modulator in VHDL is to reduce the design time and to optimize different design parameters effortlessly. Also at the same time VHDL based design can be easily be downloaded in FPGA to make it a ASIC.

Keywords: CDMA, DSSS, VHDL, FPGA.

I. Introduction:

Multiple access Techniques are used to allow many users to use the same bandwidth at the same time in most competent manner. As the spectrum is inadequate, sharing of the spectrum is then required to increase the user capacity of any wireless network by allowing the available bandwidth to be used at the same time by a no of users [1]. And this must be done in a way such that the quality of service remains the same within the existing users. CDMA is one of such spectrum efficient scheme. In Code Division Multiple Access (CDMA) scheme, many users can transmit and receive data concurrently using the same channel [2]. CDMA system offers many attractive advantages such as high spectral capacity so that it accommodates more users per MHz of bandwidth; it uses the soft hand off, rejection narrow band interference [3]. In CDMA, the same frequency can be used in every cell, because of the use of pseudo-random codes etc. One of the main advantage of CDMA is that dropouts occur only when the phone are at least twice as far from the base station. So, it is mainly used in the rural areas where GSM cannot cover the entire range. CDMA techniques are based on spread spectrum communications, which was basically used
for military applications [2-3]. In spread spectrum system the transmission bandwidth is much wider than the bandwidth of the original signal. In a CDMA communications system, a unique binary code is assigned for each call to every user. The user’s signal is multiplied by the particular code and spreading occurs to a bandwidth much wider than the original signal. All the active users share the same frequency spectrum simultaneously [4]. Spreading codes or spreading sequences can be divided into two categories such as pseudo-noise (PN) codes and orthogonal codes 3 [5-6]. PN codes are pseudo-random codes generated by shift register and XOR gates.

II. Design of CDMA Transmitter:
This paper is focused on the design of a CDMA Transmitter. We present a step by step procedure for the design. Figure 1 shows the block diagram of a CDMA transmitter. The input data signal, is multiplied with the output of a Gold pseudorandom sequence generator, in order to obtain a spread spectrum (SS) signal, which is modulated using BPSK modulation technique. The clock and control circuit drives different clock signals from the master clock.

The Gold Code Generator: The important block of DS-CDMA system is the PN sequence generator. A Gold code, also known as Gold sequence, is a type of binary sequence, used

Figure 1: Block Diagram of the CDMA Transmitter

Figure 2: Generation of Gold code and coded signal
are taken and the exclusive-ors of the two sequences gives the Gold code. The length of the Gold Sequence is $2^n - 1$. If the LSFRs are chosen appropriately, Gold sequences have better cross-correlation properties than maximum length LSFR sequences. The highest absolute cross-correlation in the set of codes is $2^{(n+2)/2} + 1$ for even $n$ and $2^{(n+1)/2} + 1$ for odd $n$ [6]. In this paper two 3 bit LFSR are implemented. Hence the length of gold sequence generated is 7.

In Order to obtain the coded signal the gold code is XNORed with the user signal.

The internal block diagram for gold code generation and generation of coded signal is given in figure 2. The coded signal is passed through a level shifter to shift the level from 1.2V to 5V. Finally the baseband signals are used to modulate the carrier sine wave to obtain the BPSK output. The BPSK modulator produces the band pass spread

Figure 3: Block Diagram of the BPSK Modulator

Figure 4: Technology Schematic

Figure 5: Layout of CDMA Transmitter
spectrum signal which is suitable for transmission from the spreaded signal. The overall block diagram of the BPSK modulator and technology schematic is given in figure 3 and figure 4 respectively. Layout of the CDMA transmitter is given in figure 5.

III. Results:
This design method requires less components for implementation and provides better simulation results. The transmitter circuit has been were coded using VHDL. Figure 6 represents the overall output of the CDMA transmitter showing user data signal, gold code, coded signal and BPSK modulated output. The average connection delay for this design is: 1.465ps

![Figure 6: Output of the CDMA transmitter](image)

Simulated result for the CDMA transmitter is shown in table 1.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>value</th>
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<tbody>
<tr>
<td>The maximum pin delay</td>
<td>3.937ps</td>
</tr>
<tr>
<td>Average connection delay on the 10 worst nets</td>
<td>1.795ps</td>
</tr>
<tr>
<td>Total estimated power consumption</td>
<td>500mW</td>
</tr>
<tr>
<td>The power consumption for Vccint=1.20V and I=100mA</td>
<td>120mW</td>
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</tbody>
</table>
IV. Conclusion:
The proposed work show a design of CDMA modulator with 120mW of power consumption with 3.937psec delay. The CDMA modulator is implemented using VHDL which is useful to implement the whole circuit in FPGA to make a ASIC. At the same time as the circuit is designed using VHDL and FPGA there is a good prospect of making a programmable hardware as because the circuit can be changed any time by changing the VHDL code. So without changing the hardware, by only changing the code we can make a new GOLD code generator which creates a new CDMA transmitter. This proposed design can be further extended for implementation of multiple transmitters. It can be implemented with different modulation techniques like PSK, QPSK, MSK and a comparative study could be done.

References: