ISSN No: 2309-4893
International Journal of Advanced Engineering and Global Technology
Vol-03, Issue-07, July 2015

Signal Integrity-A Visionary Approach

R Bhanu Kishore Singh, P Srichandraja Srihamsini

Electronics and Communication Department, GITAM University

Rudraram, Hyderabad, Telangana, India

bhanukishore29@gmail.com,chandraja.gr8@gmail.com

Abstract: **In the process of globalization, today's world has become much closer with the immense growth of communication aids. There is a huge demand for the quick, reliable and rapid transmission of data. Since the advent of electronics, the size of the technology used in the design of any electronic device has been lowering. In this era of nanotechnology, the high speed and high accuracy at low cost of data transmission has become an important requirement. All these aspects lead to the difficulty in designing for optimal signal integrity of a circuit and its consequences are very tough to realize, analyze, understand and resolve. Signal integrity has gained huge importance in the designing of any PCB circuit, whose effects are to be minimized to a maximum extent.**

I. INTRODUCTION

In electronic equipment, signals are used to carry information. At one extreme, information may be relatively simple and change slowly with the time, while at the other extreme; information may be complex and change very rapidly with the time. **Signal integrity** or SI is a set of measures of the quality of an electrical signal. In digital electronics, a stream of binary values is represented by a voltage (or current) waveform. A digital signal with good integrity has clean, fast transitions, stable and valid logic levels, accurate placement in time. If the signal integrity in a system is degraded, vital information may be lost, resulting in the system malfunction. Technological developments and market trends are pushing electronic systems to ever increasing complexity and operating speeds which places ever increasing demands on signal integrity. All parts of the system may degrade the signal integrity, which includes all the media the signal travels through, such as interconnection wires, PCB tracks etc. At low frequencies, the signals remain within the data characterization and the system performs as designed. But as system speeds increase, the higher frequency impacts on the system are not only concerned with the digital properties but the analogue effects within the system must also be considered.

II. WHY AND WHERE DOES SIGNAL INTEGRITY ISSUES ARISE?

Importance of PCB interconnects techniques increase with increase in the frequency of operation. Signal integrity is becoming an increasingly important element of the circuit and PCB design. As the frequencies used within the digital circuits rise, even comparatively short connections act as transmission lines. Signal integrity maintenance is the major issue for any high speed circuit design. At lower frequencies, a trace exhibits mostly resistive characteristics *i.e.,* just as a conductor of electrons. As the frequencies increase, *i.e.,* at mid-band frequencies, a trace begins to exhibit the characteristics of a capacitor. At higher frequencies, a trace's inductance plays a major role. At very high frequencies, the trace acts like an antenna. These variations in the characteristics at different frequencies affect the signal integrity and in turn the improper signal transmission takes place from one

part of the circuit to the other part. The 4 T's- Technology, Topology, Termination and Transmission line parameters in the design and layout of a circuit in the PCB decide the success or failure of a circuit with regard to the signal integrity. Since the signals travel through all kinds of interconnections inside a system, any electrical intact happening at source end, along the path or at the receiving end will have great effect on the signal timing and quality. Through the solder bumps of the chip package, signals go to the PCB level. The chip packages, PCBs, as well as cables and connectors form different levels of packaging systems. The typical interconnects such as metal traces, vias, power plane, ground plane which form electrical paths to conduct signals. These interconnections ultimately influence the signal integrity of the system. As the rise time gets shorter and clock frequencies get faster, connectors and cables once considered electrically transparent can have a significant effect on a system's transmitted signal. With the scaling of technology below 0.15 micrometer, the wire delays have become comparable or even greater than gate delays. In nanometer technologies at 0.13 micrometer and below, unintended interactions between signals (example: crosstalk) become an important consideration for digital system designs. Integrity loss happens when voltage distortion (noise) and delay violations (skew) go beyond an acceptable threshold. Threshold depends on the technology used in the fabrication. Such violations occur due to process variations that cause parasitic values (transistor dimensions, values of parasitic R/L/C, transmission line effects, coupling effects among interconnects which are not easy to analyze and are subject to change during fabrication.

III. SIGNAL INTEGRITY ANALYSIS

A digital system can be examined at three levels of abstraction: logic, circuit theory, and electromagnetic (EM) fields. The logic level, which is the highest level of those three, is where SI problems can be easily identified. The circuit theory specifies the design or modelling of a circuit. EM fields, located at the lowest level of abstraction, comprise the foundation that the other levels are built upon.

With the wide range of development in the field of software, there are certain software tools developed for the analysis of the issues that are created in the process of designing any PCB circuit on board. The Tools used for SI analysis Allegro PCB SI/PI, Ansoft HFSS, and Hyper Lynx Simulation Software. There are few ways of analyzing the signal integrity issues which are specified below which make the task of the designer easier and also helps in expecting the possible outcomes of a desired schematic representation.

Pre and Post layout analysis:

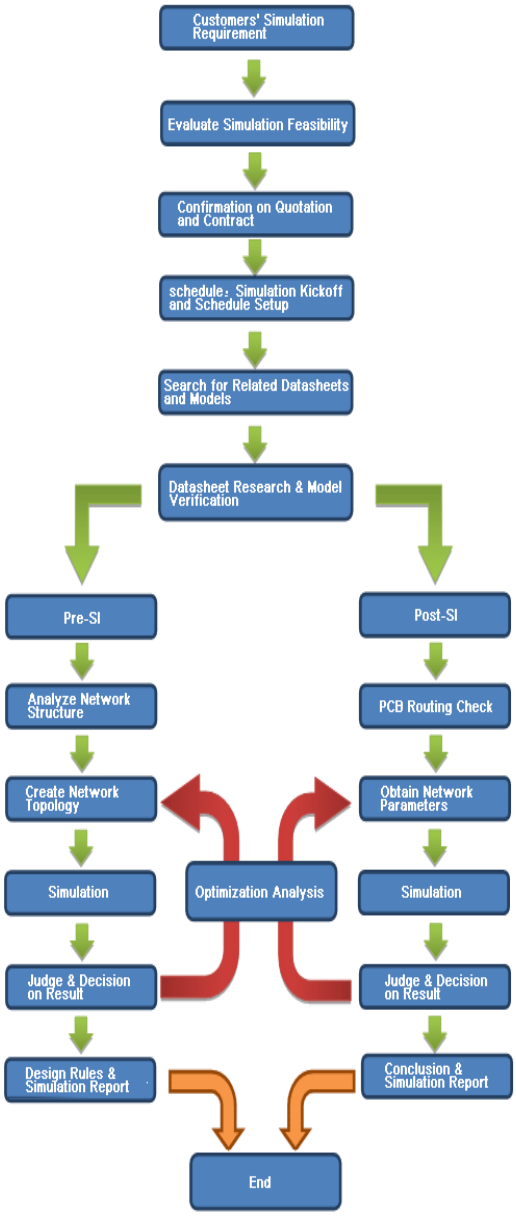
Success in electronic design often hinges on running simulations. Whether signal integrity, power integrity, electromagnetic compatibility, analog, or even thermal simulations, they reveal information about feasibility in the design and almost reduce the laborious job of on-board designing which might give undesired or inappropriate results. For example, pre-layout simulation could help determine the maximum length of a serializer/deserializer (SERDES) signal by varying the length of the trace until there's a closed eye diagram at the receiver. Post-layout simulation is used to verify the completed design. It involves extraction of physical information from the routed board. Finding a problem early in the design cycle using post-layout simulation is still orders of magnitude less expensive than trying to fix a shipping product.

Various simulations are done in both the techniques individually.

The pre analysis steps include creating network topologies, simulation, judging and making decisions, fixing the design rules and making a report.

Post analysis steps include PCB routing check, obtaining network parameters, simulation and remaining steps in procedure are same as in pre analysis.

This is explained using a flowchart as follows:

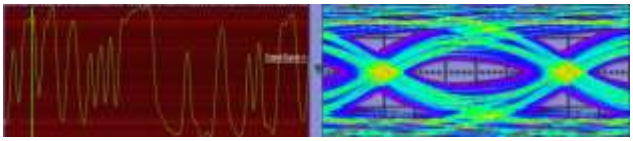


Another analysis is the Eye diagram analysis which is done apart from previous analysis.

Eye Diagram Analysis:

Eye diagram shows a number of samples within one time period. From the eye diagram we can get the successful sampling time, noise tolerance, amount of distortion. It explains intersymbol interference problems which result in distortion of signal.

The eye diagram pattern is shown as follows:



IV.PREREQUISITES FOR SI ANALYSIS

The term Signal Integrity (SI) addresses two concerns in the electrical design aspects – the timing and the quality of the signal. The goal of signal integrity analysis is to ensure reliable high-speed data transmission. In a digital system, a signal is transmitted from one component to another in the form of logic 1 or 0, which is actually at certain reference voltage levels. Any delay of the data or distortion of the data waveform will result in a failure of the data transmission.

In SI analysis, since the electric models for many interconnects can be treated as transmission lines, it is important to understand the basics of transmission line theory and get familiar with common transmission line effects in high-speed design.

Types of Transmission lines:

Micro strip line transmission line-It consists of copper trace separated from a ground plane by an insulating substrate. Since one side of conductors is exposed to air, these lines can only exist on top and bottom PCB layers.

Strip line transmission line-It is fully contained within a substrate which is sandwiched between two ground planes. Due to substrate impregnated nature of strip line, these transmission lines can exist only on internal routing layers and require a minimum of three board layers (two ground planes and a routing layer).

The study of signal propagation through these transmission lines can be made more elaborate by comprehending the modes in which signal propagation takes place. These modes affect the signal propagation in each type of transmission line respectively.

Even and Odd modes of propagation:
When two independent micro strip lines are placed close to each other, the impact of coupling between them and their signal propagation cannot be neglected. The intended characteristic impedances of two lines are affected by their relative switching characteristics. This leads to even and odd modes of propagation. When the pair is driven is with complementary signals (equal amplitude and 180° out of phase), it is said to be an odd mode and if the pair is driven with signals in phase with each other is said to be an even mode. In an odd mode the mutual capacitance is maximized whereas mutual inductance is maximized in the case of an even mode.

V. TYPICAL SI PROBLEMS:

"Timing" is everything in a high-speed system. Signal timing depends on the delay caused by the physical length that the signal must propagate. It also depends on the shape of the waveform when the threshold is reached. Signal waveform distortions can be caused by different mechanisms. But there are three mostly concerned noise problems:

• Crosstalk Noise Due to electromagnetic coupling between signal traces and vias.

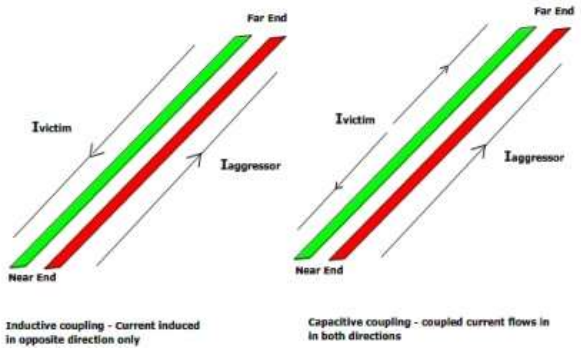
• Reflection Noise Due to impedance mismatch, stubs, vias and other interconnect discontinuities.

• Power/Ground Noise Due to parasitics of the power/ground delivery system during drivers' simultaneous switching output (SSO). It is sometimes also called Ground Bounce, Delta-I Noise or Simultaneous Switching Noise (SSN).

Besides these three kinds of SI problems, there are other Electromagnetic Compatibility or Electromagnetic Interference (EMC/EMI) problems that may contribute to the signal waveform distortions. When SI problems happen and the system noise margin requirements are not satisfied – the input to a switching receiver makes an inflection below Vih minimum or above Vil maximum; the input to a quiet receiver rises above Vil maximum or falls below Vih minimum; power/ground voltage fluctuations disturb the data in the latch, then logic error, data drop, false switching, or even system failure may occur. These types of noise faults are extremely difficult to diagnose and solve after the system is built. Understanding and solving these problems before they occur will eliminate having to deal with them further into the project cycle, and will in turn cut down the development cycle and reduce the cost. A brief explanation of the effects of signal integrity is discussed below as follows:

Crosstalk (XT):
Crosstalk (XT) is a disturbance caused by the electric or magnetic fields of one telecommunication signal affecting a signal in an adjacent circuit. In a telephone circuit, crosstalk can result in your hearing part of a voice conversation from another circuit. It can occur when long traces running next to each other coupled their signals together through mutual capacitance and inductance. It can cause noise pick up on the adjacent quiet signal lines that may lead to false logic switching.

Forms of crosstalk:
There are two nets or traces considered. One is the aggressor net and the latter one is the victim net. Due to the magnetic action of aggressor net there is an effect in the neighboring net which is hence called as victim net. These two traces or nets are coupled magnetically.These traces are either inductively coupled or capacitively coupled which causes the current direction to vary in each case as shown.

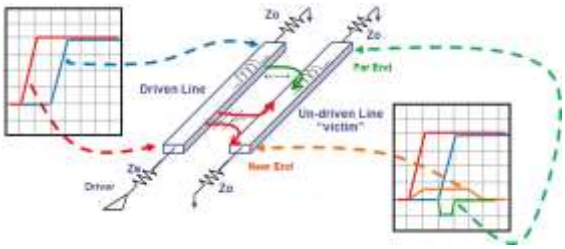


There are two different ways in which crosstalk appears:

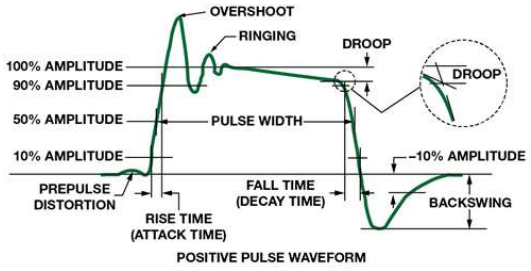
NEXT (Near End or Backward/Reverse Cross Talk):
Portion of coupled energy that flows (within the

victim net) opposite to the direction of the aggressor signal.

FEXT (Far End or Forward Cross Talk): Portion of coupled energy that flows (within the victim net) in the same direction of the aggressor signal.
The following diagram shown explains how the crosstalk takes place:



Reflections and Edge Aberrations:
Reflections can be caused by the terminations and board layout problems, where the outgoing signal bounces back towards its source and interferes with subsequent pulses. The root cause of reflection noise is the impedance mismatch, stubs, vias and other interconnect discontinuities along the signal transmission path. When a signal changes its routing layer and the impedance values are not consistent (manufacturing variations, design considerations, *etc*.,) reflection will occur at the discontinuity boundary. Edge aberrations can result from board layout problems or from improper termination or even quality problems in the semiconductor devices. Aberrations can include rounding, overshoot, ringing and slow rise time.
The diagram shown below explains single pulse transmission and various effects on the signal.



Power/Ground Noise:
Power/ground noises occupy 30%+ noise budget in today's high-speed design. Ground Bounces, caused by excessive current draw (and/or resistance in the power supply and ground return paths), can cause a circuits ground reference level to shift when current demands are high. It will cause logic error when it couples to quiet signal nets or disturbs the data in the latch. It may introduce common mode noise in mixed analog and digital design. With ever-increasing IC transition speed and I/O count, packages with new emerging technologies are capable of switching under 200 picoseconds transition time and sinking up to 20 Amperes of power supply current. The SSN increases significantly as this trend continues.

EMI-Electromagnetic Interference:
It is electromagnetic radiation that causes undesired responses or degradation of performance in electronic equipment.

EMC-Electromagnetic Compatibility
It defines the capability of equipment to be used in their intended environment without causing degradation due to undesired EMI.
Hence EMC helps in determining the limits for equipment that has to be designed which would be free from emitting radiations that cause departure in SI. The timing of the signal also plays a major role in creating problems pertaining to SI. There are certain requirements for a signal pulse that has to be transmitted and is expected to go variations ideally as per the defined terminology as mentioned below.

Set-up Time: A clocked device, such as D-Flip-flop requires the data to be stable at its input for a specified time before the clock arrives. This is known as Setup-Time.
Hold Time: Similarly the input data must remain valid for a specified time after the leading edge of clock.
These two requirements are not satisfied in real time systems which causes timing problem.

Jitter: Jitter is defined as edge placement variations from cycle to cycle. Some important causes of jitter are noise, crosstalk and timing instability. This can affect timing accuracy and synchronization throughout a digital system.

VI. POSSIBLE SOLUTIONS

The challenges of high-speed design require some additional effort to ensure signal integrity. This can

be achieved by following some simple analogue design rules and by using careful PCB layout techniques. Few techniques are discussed as follows:

• *Differential signaling system:*
A differential signaling system is one where a signal is transmitted down a pair of tightly coupled carriers, one of these carrying the signal, the other carrying an equal but opposite image of the signal. Differential signaling was developed to cater for situations where the logic reference ground of the signal source could not be well connected to the logic reference ground of the load. Another major advantage of differential signaling is that it minimizes electromagnetic interference (EMI) generated from the signal pair.

• Few techniques to control the crosstalk are one can make the lines space apart, add ground guarding band in between the signal lines, keep the parallelism to minimum, and keep the traces close to the reference metal planes.

• Reflections can be minimized by maintaining proper impedances at the output with predetermined values by proper analysis.

VII. CONCLUSION

Degradation of signal integrity is the most common issue which needs special attention for effective data transmission. In the recent trends, the high speed demands that are required must overcome the effects of signal integrity by effective analysis and predetermination of erroneous cases. There are certain methods discussed which can be the possible solutions to resolve these issues to a maximum extent, albeit not ideally, and working on these impacts can lead to the development of new techniques to diminish these effects which results in efficient data transmission at higher speeds. Scientists have taken a step ahead to minimize these effects and yield maximum accuracy by developing various software tools using which the pre and post analysis of the PCB circuit would become designer friendly and economical, instead of directly going into a 'practical implementation' of the desired logic design on the board. This is an endeavour of a researcher in the present PCB design scenario so that the future technology works stands good devoid of even an iota of a flaw in data transmission.

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