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Quality Improvement of Image Edge Detection, leading to the Accelerator

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Abstract :- **Edges characterize boundaries, which relates to a prime necessity in design of an Image processor. Edge detection of an image significantly reduces the quality of information and filters out useless information, while preserving the structural properties.**

Our paper consists of a novel algorithm for Sobel and Prewitt edge detection accelerator, which give improved results compared to traditional methods. The speedup of the accelerator is explained by using Amdahl's law.

The novel algorithm has been applied for both grayscale and colour images, which performs enhanced simulation output in respect of Mean Square Error (MSE) and Peak Signal to Noise Ratio (PSNR).

Our work has used the coefficient file for implanting in IP Core generator which being well designed for the hardware implementation of our accelerator.

Key Words :- Sobel, Prewitt, Amdahl's law, Coefficient file, MSE, PSNR, IP core generator.

I. INTRODUCTION

In modern days, to keep pace with the rapid progressing of technologies, we have to make everything faster, that's where accelerator enters into the technology. Accelerators accelerate the performance of devices. Edge detection accelerators speed up the edge detection processes. Edge detection refers to the process of identifying and locating sharp discontinuities in an image. The discontinuities are abrupt changes in pixel intensity which characterize boundaries of objects in a scene. Classical methods of edge detection involve convolving the image with an operator (a 2-D filter), which is constructed to be sensitive to large gradients in the image while returning values of zero in uniform regions. There are an extremely large number of edge detection operators available, each designed to be sensitive to certain types of edges. Some Edge detection operators are – Sobel, Prewitt , Canny , Roberts operator etc. In this paper, the work is done mainly on Sobel and Prewitt operators. These are mainly Gradient Edge detection methods. Our work illustrates different approaches to design a hardware accelerator based on Sobel and Prewitt edge detections.

A. Literature survey :

Edge detection is required for Video segmentation [1] . Video Segmentation is the basic requirement for applications such as video surveillance, traffic management and medical imaging. The high computation power must be provided to support this operation. Sobel edge detection operator is used to design the hardware for video segmentation. Adaptive edge detection [2,3] is required for Real time video processing using FPGA. Real-time video and image processing is used in a wide variety of applications from video surveillance and traffic management to medical imaging applications. High computation power is required for this. We can detect a real time 3D object by its Edge and depth information [4]. As FPGA gives higher flexibility, design of hardware accelerator using FPGA is more advantageous. According to the paper [5] , Video processing has been used in many fields such as industry, military, medical image processing, surveillances recording etc. Video and imaging applications demand a range of processes to be performed in single applications. Edge detection is one of the basic characteristics of the image. It is an important basis for the field of image analysis such as: the image segmentation, target area identification, extraction and other regional forms .It is widely used in image segmentation, image recognition, and texture analysis of them. Edge detection technology not only detect the image gray value of the non-continuity, but also to determine their exact location . Edge detection is the foundation of pattern recognition [6]. Especially, in noisy images Edge detection is more important because noise is a common phenomenon in image. Edge

detection is mainly dependent on the intensity changes in the different images [7]. In [7] , it also computes about the scalability of the natural images, which follows the laplacian and Gaussian distribution. In the paper [8,12], a comparison between various image edge detection techniques has been discussed. According to this paper, Edge detection techniques are generally of two types as- 1) Gradient based edge detection and 2) Laplacian based edge detection. The paper [9] introduces with the method of image processing using IP Core Generator through FPGA. According to this paper, Block Memory Generator provides single port and dual port block memory. These memory types differ in selection of operating modes. Matlab tool is used to convert the image that is being processed to .coe file format. Xilinx Core Generator is used to store the coefficient file(.coe) in single port Block ROM by defining the width and depth of the image and image is displayed on VGA monitor using FPGA board. The paper [10] shows the Real time edge detection modelling using FPGA. According to this paper, design of hardware based on edge detection can be done by some user defined peripherals and interfaces in Xilinx Core Generator. The paper [11] proposes an auto-adaptive edge detection algorithm, which acts as a measure for image- based fire monitoring, early fire detection, fire evaluation and determination of other parameters related to flame and fire image. The process of identifying a boundary between the area where there is thermo-chemical reaction and those without, leads to determination of flame and fire edges. Boundary detection of medical images can also be done using edge detection based on Intensity gradient and texture gradient features [13]. A proposal for the method of robust detection of abandoned and removed objects in complex surveillance videos have been illustrated [14]. It is important for anti-terrorism movement. The paper [15] proposes the design of hardware / software FPGA based system for fast image processing. It proposes different modules of filters, which finally helps in the designing of an accelerator. In [16-18] provides an idea about different edge detection parameters such as MSE(Mean square error), PSNR(Peak signal to noise ratio) and also different statistical parameters.

B. Overview:

The rest of the paper is organized as follows. In Section 2 the basic concepts of adopted edge detections are presented. In Section 3 we present the edge detection architectures used, while Section 4 presents some experimental results. Section 5 presents the hardware design. Finally Section 6 concludes the paper.

II. EDGE DETECTION TECHNIQUES

In this section, we have discussed about different edge detection techniques. We have followed edge detection technique using two most popular operators i.e. Sobel and Prewitt operators.

A. Sobel Operator :

The operator consists of a pair of 3×3 convolution kernels as shown in Figure 1. The two kernels (G_x and G_y) is correlated to each other by a rotation of 90° along both vertical and horizontal directions.

+1	+2	+1
0	0	0
-1	-2	-1

G_x

-1	0	+1
-2	0	+2
-1	0	+1

G_y

Fig.1: Masks used by Sobel Operator

These kernels are designed to respond maximally to edges running vertically and horizontally relative to the pixel grid. The kernels can be applied separately to the input image, to produce separate measurements of the gradient component in each orientation (call these G_x and G_y). These can then be agglomerated together to find the absolute magnitude of the gradient at each point and proper orientation of that gradient. The gradient magnitude is given by:

$$|G| = \sqrt{G_x^2 + G_y^2}$$

Typically, an approximate magnitude is computed using:

$$|G| = |G_x| + |G_y| \;;$$

which is much faster to compute.
The improved angle of orientation of the edges gives rise to the spatial gradient (relative to the pixel grid orientation) and it is given by:

$$\theta = \arctan(G_y / G_x) - 3\pi / 4.$$

B. Prewitt Operator :

Prewitt operator follows identically all the computational procedures in respect of sobel operator except the kernels G_x and G_y , which are redefined as follows:

+1	+1	+1
0	0	0
-1	-1	-1

G_x

-1	0	+1
-1	0	+1
-1	0	+1

G_y

Fig.2: Masks used by Prewitt Operator

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III. ARCHITECTURE OF EDGE DETECTION

Accelerator acts as a co-processor for the embedded architecture, which speed up the performance of the processor. As discussed by Amdahl's law, the speedup of a processor is given by:

$$s' = \frac{t}{t'} = \frac{ft + (1-f)t}{\frac{ft}{s} + (1-f)t} = \frac{1}{\frac{f}{s} + (1-f)}$$

where, s'= overall speedup, s= speedup factor, f= fraction of time used for execution of the kernel, t= time spent.

We have obtained two major edge detection architectures while designing our accelerator as discussed below.

A. Sobel Accelerator Architecture :

The architecture for the Sobel accelerator datapath is shown in Fig.3. It is essentially a pipeline, with pixel data read from the original image entering into the registers at the top right, flowing through the 3×3 multiplier array on the left, then down through the adders to the D_x and D_y registers, then through the absolute value circuits and adder to the |D| register, and finally into the register at the bottom left. The resulting derivative pixels are then written from that register to memory. (While a right-to-left data flow is opposite to usual practice, in this case, it has the advantage of preserving the same arrangement of pixels as that in an image.)

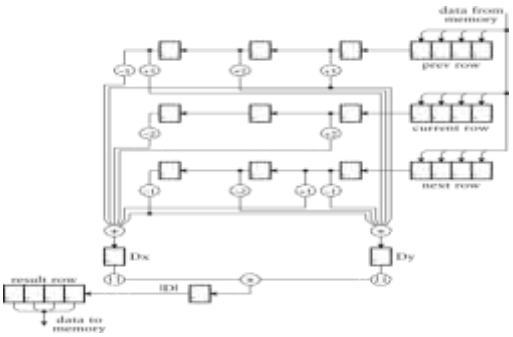

Fig.3: Sobel Accelerator Architecture

B. Prewitt Accelerator Architecture :

The architecture for the Prewitt accelerator datapath is shown in Fig.4. The operation of data path is same as Sobel Accelerator Architecture.

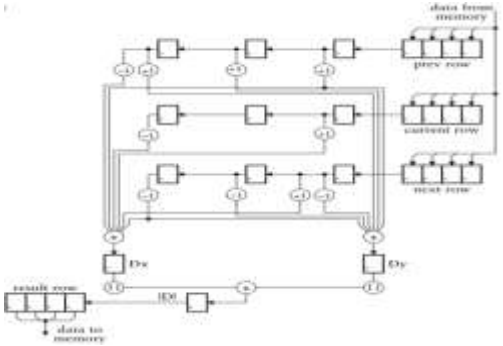

Fig.4: Prewitt Accelerator Architecture

C. Matlab pseudo-code :

```
function img2=sobel_edge('image_file')
variable1 = imread('image_file'); \..read image..\
\..get the dimensional informations i.e. height, width, channel
of the image..\
imgOutput = zeros(size('image_file')); \.. output image..\
Gx = \.. Horizontal mask matrix..\ ;
Gy = \..Vertical mask matrix..\;
for i = 2 : height - 1
 for j = 2 : width - 1
 for k = 1 : channel
 variable2 = variable1(i - 1 : i + 1, j - 1 : j + 1, k);
 x = \..matrix multiplication of Gx and variable2..\ ;
 y =\..matrix multiplication of Gy and variable2..\;
 variable3 = square-root of (square of x +square of  y);
        imgOutput(i, j, k) = variable3;
 end
 end
end
figure;
imshow(imgOutput);
title('Sobel Edge Detection');
% original image
figure;
title('Original Image');
```

IV. EXPERIMENTAL RESULTS

Here we have obtained the simulation results from the sobel and prewitt edge detection methods as discussed in section II. The process for edge detection methods by using the kernel G is explained in Fig.5

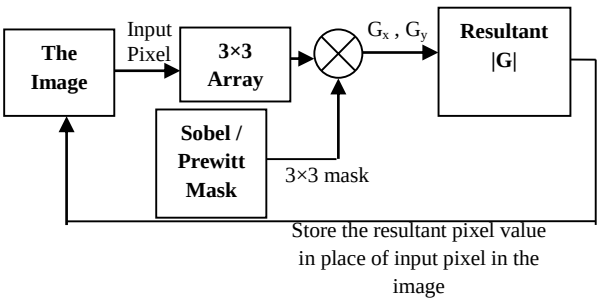

Fig.5: Block diagram of edge detection

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A. Simulation Results :

The results found from the novel algorithm are better than the results found from traditional method. The different results are shown below:

Fig.6(a): Original Image (330×330)

Fig.6(b): novel algorithm

Fig.6(c): traditional method

Fig.7(a): Original Image(230×230)

Fig.7(b): novel algorithm

Fig.7(c): traditional method

Fig.8(a): Original image(560×400)

Fig.8(b): novel algorithm

Fig.8(c): traditional method

Fig.9(a): Original Image(800×600)

Fig.9(b): novel algorithm

Fig.9(c): traditional method

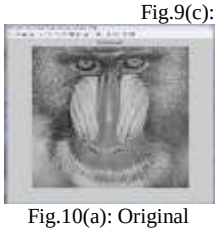

Fig.10(a): Original Image(1024×1024)

Fig.10(b): novel algorithm

Fig.10(c): traditional method

Fig.11(a): Original Image(1024×768)

Fig.11(b): novel algorithm

Fig.11(c): traditional method

How the images are improved using the novel algorithm from the traditional method is measured using the calculation of MSE and PSNR.

Now, the MSE and PSNR of the images has been calculated using following formulas-

$\text{MSE} = \frac{1}{\text{NM}} \sum_{\text{m}=0}^{\text{M}-1} \sum_{\text{n}=0}^{\text{N}-1} \text{e}(\text{m}, \text{n})^2$; where e(m,n) is the error differences between original and distorted image.

$\text{PSNR} = 10\log \frac{s^2}{\text{MSE}}$; where s=255 for an 8 bit image.

Original Image	Novel Algorithm		Traditional Method	
	MSE	PSNR(dB)	MSE	PSNR(dB)
Fig.6(a)	232.9	24.493	248.43	24.213
Fig.7(a)	74.59	29.438	81.86	29.034
	74.89	29.421	81.99	29.027
	75.23	29.401	82.06	29.024
Fig.8(a)	96.57	28.326	165.21	25.984
Fig.9(a)	34.09	32.838	46.83	31.459
	28.49	33.618	41.18	32.018
	30.20	33.364	44.30	31.701

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Fig.10(a)	183.1	25.536	230.58	24.537
Fig.11(a)	68.44	29.812	79.76	29.147
	62.32	30.218	75.97	29.358
	60.60	30.340	70.80	29.665

Table.1: Comparison of MSE and PSNR

Table.1 shows that the MSE is lesser in novel algorithm than the traditional method. The PSNR is also improved in the novel algorithm.
Table.2 shows the timing comparison between the novel algorithm and traditional method for a image (Fig. 7(a)).

No. of Iterations	Execution time	
	Novel Algorithm	Traditional Method
1	1.5046s	0.3512s
2	1.5092s	0.3557s
3	1.4903s	0.4266s
4	1.4826s	0.4137s

Table.2: Comparison of execution time

V. HARDWARE DESIGN

The hardware design is done using sobel and prewitt architecture (Fig.3, Fig.4) and the edge detection block diagram (Fig.5). The first approach towards the design is taken using HDL language. A 3×3 array and a 6×6 array of pixels are taken for the implementation of the architecture.

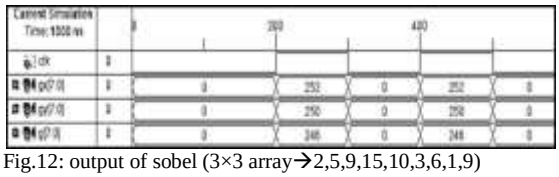

Fig.12: output of sobel (3×3 array→2,5,9,15,10,3,6,1,9)

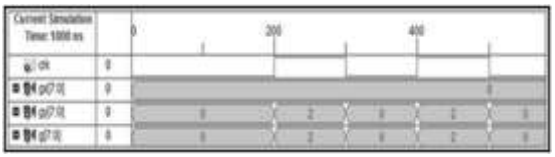

Fig.13: output of prewitt (3×3 array→2,5,9,15,10,3,6,1,9)

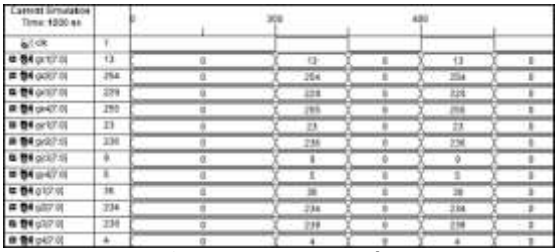

Fig.14: output of sobel (9×9 array→1,2,7,3,14,10,5,6, 8,11,0,5,4,1,0,9,1,3,5,9,14,10,5,10,5,0,5,8,4,7,0,1,10,15,3,1)

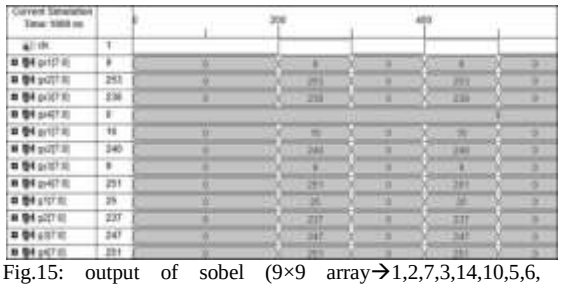

Fig.15: output of sobel (9×9 array→1,2,7,3,14,10,5,6, 8,11,0,5,4,1,0,9,1,3,5,9,14,10,5,10,5,0,5,8,4,7,0,1,10,15,3,1)

In the above results the unsigned values are taken. The hardware requirement is follows-
For 3×3 array→

Sobel :		Prewitt :	
# ROMs	: 8	# ROMs	: 8
9x12-bit ROM	: 4	9x4-bit ROM	: 8
9x8-bit ROM	: 4	# Multipliers	: 12
# Multipliers	: 12	4x2-bit multiplier	: 12
4x4-bit multiplier	: 12	# Adders/Subtractors	: 18
# Adders/Subtractors	: 18	4-bit adder	: 7
4-bit adder	: 7	8-bit adder	: 9
8-bit adder	: 9	8-bit subtractor	: 2
8-bit subtractor	: 2		

For 9×9 array→

Sobel :		Prewitt :	
# ROMs	: 56	# ROMs	: 56
36x8-bit ROM	: 48	36x8-bit ROM	: 48
9x4-bit ROM	: 4	9x4-bit ROM	: 4
9x8-bit ROM	: 4	9x8-bit ROM	: 4
# Multipliers	: 48	# Multipliers	: 48
8x4-bit multiplier	: 48	8x4-bit multiplier	: 48
# Adders/Subtractors	: 72	# Adders/Subtractors	: 72
12-bit adder	: 32	12-bit adder	: 32
6-bit adder	: 28	6-bit adder	: 28
12-bit subtractor	: 8	12-bit subtractor	: 8
8-bit adder	: 4	8-bit adder	: 4

The hardware design is done using Xilinx Core generator also. The block diagram is shown in Fig.16.

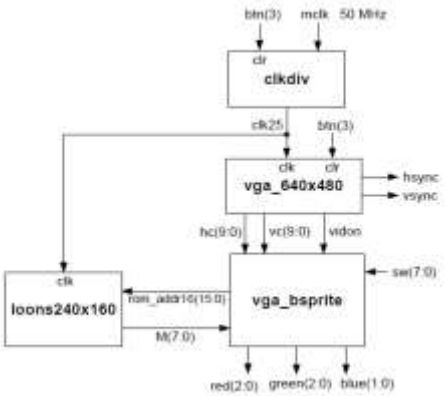

Fig.16: Top level design

The output can be seen in VGA screen. The output is generated from .coe file, which consists of upper 3 bits of red, 3 bits of green and 2 bits of blue. We have designed above blocks using Xilinx. The input image is loons 240×160. It is converted into coefficient file (.coe). Then that .coe file is loaded into a single port block memory shown in Fig.17

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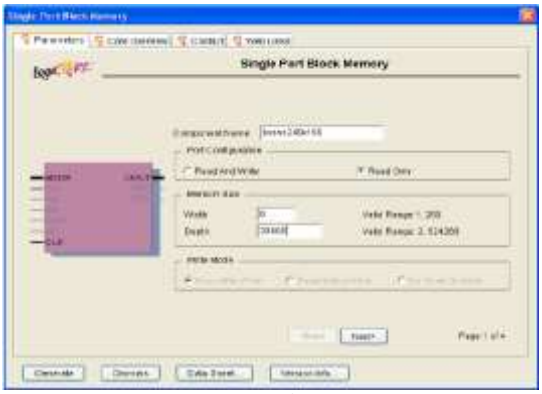

Fig.17: Generating of the component

VI. CONCLUSION

Due to rapid progress in the field of VLSI technology now the devices are faster than before. The proposed accelerator circuit is implemented in such way that it can fit to the latest trends. If any novel implementation is possible then that will be optimum achievement in this field of project work. We are concerned more about the circuit speed, noise immunity and power consumption. In present era, low power consumption is the most important characteristics for any kind of circuit-level implementation. This accelerator can be used in medical image processing, security purposes such as Face detection, Finger print detection etc.

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